REMARKS

Rejections under 35 USC §103(a)

Claims 1, 2, 4, 5, 7-9 and 13-16 were rejected under 35 USC §103(a) as being obvious over Matsunaga (U.S. Patent No. 6,670,710 B2) in view of Vigna et al. (U.S. Patent No. 6,605,873 B1).

Claim 1 has been amended to recite "said first multilayer interconnection structure including a pillar vertically extending straight from a surface of said substrate and reaching at least said second multilayer interconnection structure, said pillar being formed in a region of said substrate right underneath an electrode pad."

In the Office Action, the Examiner alleged that Matsunaga discloses "a pillar (30) extending from a surface of said substrate and reaching at least said second multilayer interconnection structure." The Examiner also alleged that "it would have been obvious . . . to modify the pillar structure of Matsunaga by forming it on a device isolation structure and beneath an electrode pad as taught by Vigna to distribute stress from the device regions of the substrate to the device isolation regions during a wiring bonding process."

Matsunaga describes that "As shown in FIG. 1, **a via ring 30 is formed along the periphery of a chip 10**. The via ring 30 surrounds the device area of the chip 10." (Col. 4, line 13-16). Thus, reference numeral 30 which appears like a pillar in Figs. 2-11 is a via ring.

Thus, Matsunaga does not disclose a pillar. The term "pillar" must be interpreted in an ordinary meaning. "Webster's Encyclopedic Unabridged Dictionary" defines as follows:

> 1. an **upright shaft** or structure, of stone, brick or other material, **relatively slender in proportion to its height** and of any shape in section, used as a building support, or standing alone as for a monument: Gothic pillars; . . . .

Thus, according to the ordinary meaning, "pillar" is "an upright shaft" or structure "relatively slender in proportion to its height." The via ring 30 extends along a periphery of a square shape as shown in Fig. 1 of Matsunaga. What Matsunaga discloses is rather a long "wall" than a "pillar" compared to the present invention.

As the Examiner admits, in Matsunaga, the via ring is not formed in a region of the substrate right underneath the electrode pad." Moreover, in Matsunaga, because the via ring is not formed in the region of the substrate right underneath the electrode, there is no electrode pad over the via ring.

Moreover, the objective of forming the via ring has nothing to do with that of the present invention. **The via ring is formed to prevent cracks at the time of scribing and the via ring 81 serves to prevent water from entering the chip from the side portions of the chip** (col. 2, line 32 to 67).

Vigna et al describes as follows:

> A second dielectric layer 18 extends on top of first metal level 13 and has openings housing C-shaped portions 19 formed starting from a second metal level 20 also forming an annular region 21. In the vertical direction, annular region 21 is substantially aligned with the peripheral portion 15a of interconnection and relief region 15 to which it is electrically and mechanically connected by means of portions 19. A third dielectric layer 23 extends on top of second metal level and has an annular opening housing an **annular portion 24** (the shape of which can be seen in FIG. 1) formed starting from a third metal level 27 also forming a pad region 28 of the device. Pad region 28 is rectangular (see FIG. 1 in particular), extends on top of third metal layer 23 and is electrically connected to annular

> bearing region 21, near its periphery, by means of annular portion 24. Finally, a passivation layer 29 covers the entire device 1 with the exception of an opening 30 at pad 28, to permit bonding of the wire(s).
> As will be noted, at the bottom, pad 28 is connected to a bearing structure 31 comprising regions 21, 15a and portions 24, 19, 12 and extending vertically entirely outside the component 3; in particular, on one side, the bearing structure 31 electrically connects the pad 28 to component 3 through portion 15b and on the other side it acts to concentrate the mechanical stress to which the pad is subjected during wire bonding on a limited peripheral area not containing electronic components or conductive regions, but only field oxide layer 6. In this way the stress exerted on component 3 during wire bonding is considerably reduced; furthermore, there are no dielectric/metal interfaces between second and third metal layers 18, 23 on top of component 3; consequently, delamination problems are eliminated in this zone.

(Col. 3, lines 5-37).

Vigna et al also discloses annular portion 24 which is made of a wall rather than a pillar. Also, the "bearing structure" does not vertically extend straight from a surface of the substrate and reaching at least the second multilayer interconnection structure. Moreover, because the "bearing structure" is of annular structure, the application will be limited to those devices which permit such annular structure around the pad.

Therefore, Matsunaga et al and Vigna et al do not teach or suggest "said first multilayer interconnection structure including a pillar vertically extending straight from a surface of said substrate and reaching at least said second multilayer interconnection structure, said pillar being formed in a region of said substrate right underneath an electrode pad," as recited in claim 1.

Moreover, as noted above, the objective of forming the via ring in Matsunaga has nothing to do with that of the present invention. Therefore, there is no suggestion or motivation to combine the teaching of Matsunaga with the teaching of Vigna et al.

For at least these reasons, claim 1 patentably distinguishes over Matsunaga et al and Vigna et al. Claims 2, 4, 5, 7-9 and 13-16, depending from claim 1, also patentably distinguish over Matsunaga et al and Vigna et al for at least the same reasons.

Claims 10-12 and 17-19 were rejected under 35 USC §103(a) as being obvious over Matsunaga (U.S. Patent No. 6,670,710 B2) in view of Vigna et al. (U.S. Patent No. 6,605,873 B1) as applied to claim 1 above, and further in view of the Applicant's Prior Art Figures 1-4 (APAF).

Claims 10-12 and 17-19, all depend from claim 1.

APAF has been cited for allegedly disclosing that a first interlayer insulating film and second interlayer insulating film each have the desired properties such as Young's modulus and porous organic film recited in the claimed invention. Such disclosures, however, do not remedy the deficiencies of Matsunaga and Vigna et al.

For at least these reasons, claims 10-12 and 17-19 patentably distinguish over Matsunaga, Vigna et al and APAF.

Claim 21 is rejected under 35 USC §103(a) as being obvious over Matsunaga (U.S. Patent No. 6,670,710 B2) in view of Vigna et al. (U.S. Patent No. 6,605,873 B1) as applied to claim 1 above, and further in view of Sugiyama et al. (US Publication No. 2002/0040986 A1).

Claim 21 depends from claim 1.

Sugiyama et al has been cited for allegedly disclosing a more detailed interconnection layout. However, such disclosure does not remedy the deficiencies of Matsunaga and Vigna et al.

For at least these reasons, claim 21 patentably distinguishes over Matsunaga, Vigna et al and Sugiyama et al.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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Enclosures: Webster's Encyclopedic Unabridged Dictionary of the English Language